Design and Analysis of Energy-Efficient High-Speed CMOS D Flip-Flops and Counters Employing Double-Gate F in FET Technology

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ABSTRACT

As semiconductor technology progresses, the need for energy-efficient digital circuits continues to rise, especially in applications such as portable devices and data centers. F in FET (Fin Field Effect Transistor) technology has emerged as a revolutionary advancement, offering enhanced control over short-channel effects, thereby minimizing power leakage and improving overall efficiency. This paper explores the design andsimulationofcountersutilizingFinFET-basedDFlip-Flopsatthe10nm technology node, implemented in LT- Spice, a popular circuit simulation tool. Compared to conventional CMOS designs, F in FET-based counters exhibit a remarkable reduction in power consumption and noise, with improvements of 57.13% and 46.02%, respectively. Additionally, asynchronous and Johnson counters implemented with F in FET technology outperform their CMOS counterparts in terms of speed and reliability. These findings affirm that F in FET technology is available solution for achieving high-speed, low-power digital circuits, making it an ideal choice for future semiconductor designs.

Keywords: FinFETTechnology, CMOS Limitations, Short-Channel Effects, D Flip-Flop Design, LT- Spice Tool, Power Efficiency, Noise Reduction, Semiconductor Advancement.

I. INTRODUCTION

Counters are essential components in digital systems, extensively used for various applications such as event counting, frequency division, timing signal generation, and control logic implementation in devices ranging from consumer electronics to high-performance computing systems. The performance and power efficiency of these counters have a profound impact on the overall functionality of digital circuits, where minimizing power consumption and enhancing operating speed are critical design goals. With the continuous scaling of semiconductor technology, conventional CMOS technology encounters limitations such as increased leakage current, higher power dissipation, and degraded performance due to short-channel effects. These challenges have prompted the adoption of FinFET (Fin Field Effect Transistor) technology, which offers superior electrostatic control, reduced leakage, and improved energy efficiency, making it an ideal solution for designing high-speed, low-power digital counters.

Researchers have implemented innovative techniques to design power-efficient circuits using F in FET-based D-Latches and D Flip-Flops (DFFs). The True Single-Phase Clock(TSPC) D Flip-Flop, widely used in high-speed digital designs, eliminates the need for setup time but introduces longer hold times, which can be mitigated using an area-power-efficient shunt capacitor technique. This technique effectively shorten should time with minimal impact on setup time, enhancing the overall performance of the DFF.

Furthermore, Johnson Counters, a modified version of ring counters, utilize a feedback loop where the output of the final flip-flop is connected to the input of the first flip- flop. This feedback mechanism allows the counter

to generate a distinct sequence of binary states, making Johnson Counters more efficient for specific counting and sequencing tasks. Ripple counters, on the other hand, offer simplicity in design but suffer from propagation delays, which limit their use in high-speed applications. This study focuses on the design and implementation of high-speed, low-power CMOS D Flip-Flops and counters using Double Gate (DG) F in FET technology. The impact of fin width (W fin) scalingbelow10nmon F in FET analog performance is extensively analyzed. Simulation results demonstrate that while reducing Wf in improves short-channel control, excessive scaling adversely affects the device transconductance(gm) and output conductance(gds), resulting in degraded analog performance. Key parameters influencing these variations include source/drain resistance (RS/D), material resistivity (ρ), and operating temperature (T), which must be carefully optimized in sub-10nm F in FETs to achieve the desired performance.

To validate the proposed design, 4-bit Johnson and Ripple counters were implemented using 45nm technology with a 1V supply voltage. The simulation results highlight a significant reduction in power consumption and propagation delay, making these designs suit able for low-power, high-speed applications.

II. EXISTINGMETHOD

The need for high-performance and energy-efficient digital circuits has increased dramatically as semiconductor technology develops. For many years, the foundation of VLSI design has been CMOS (Complementary Metal-Oxide- Semiconductor) technology. However, CMOS encounters significant difficulties such as higher power consumption, short-channel effects, and decreased performance as device dimensions decrease below20 nm. Fin FET (Fin Field-Effect Transistor) technology has become a viable substitute for these problems, offering improved performance, scalability, and energy efficiency.

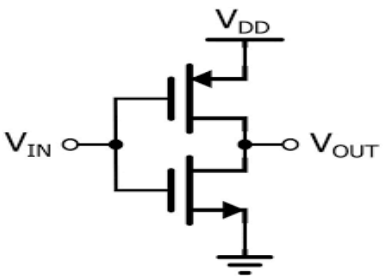

Fig:1:CMOS INVERTER

This paper examines the shortcomings of the current CMOS system, the necessity of a new system, and F in FET's potential contribution to VLSI in the future.

CMOS technology has dominated the semiconductor industry due to its low power consumption, ease of manufacturing, and maturity. It is widely used in designing logic gates, flip-flops, counters, and microprocessors. Short-Channel Effects (SCE):As transistors shrink, controlling the channel becomes difficult, leading to leakage currents and degraded performance.

High Power Dissipation: Leakage currents in smaller nodes result in increased static power consumption, which is critical for battery-powered and portable devices. Scaling Issues: Below 20nm, planar CMOS designs face physical and electrical limitations, making further miniaturization challenging.

Increased Noise: Smaller dimensions reduce noise immunity, leading to stability concerns in digital circuits.

Heat Generation: Increased leakage power results in excessive heat, affecting circuit reliability.

Higher Leakage Current: Traditional MOSFETs suffer from subthreshold leakage and gate leakage at smaller technology nodes.

Performance Degradation at Small Nodes: Below 20nm, CMOS technology becomes inefficient due to increased leakage and poor gate control.

Increased Delay: CMOS-based sequential circuits experience greater propagation delays in high- frequency applications.

Conventional D Flip-Flop CMOS:

A common design that uses two cross-coupled inverters to hold data is the conventional CMOS D flip-flop. This design's primary benefit is its simplicity, which leads to a small footprint and low power usage. Nevertheless, there are many drawbacks to the conventional CMOSD flip-flop, including its slow speed and high leakage current. The flip-flop may eventually the data it has saved due to the leakage current, which can be especially troublesome.

1. D Flip-Flop based on F in FET:

Double-gate MOSFET transistors are used in the DGMOS D flip-flop design to increase the flip-flop's speed and power consumption. Highspeed, low leakage current, and low power consumption are just a few benefits of double-gate MOSFET transistors.

2. *CMOS D Flip-Flop Static*

Two cross-coupled inverters are used in the static CMOS D flip-flop device to store data. This design's primary benefit is its simplicity, which leads toa small footprint and low power usage. Nevertheless, the static CMOS D flip-flop has many drawbacks, including a high leakage current and a restricted speed. The flip-flop may eventually lose the data it has saved due to the leakage current, which can be especially troublesome.

3. *D Flip-Flop Double-Gate MOSFET(DGMOS)*

Double-gate MOSFET transistors are used in the DGMOS D flip-flop design to increase the flip-flop's speed and power consumption. High speed, low leakage current, and low power consumption are just a few benefits of double-gate MOSFET transistors.

4. *CMOS D Flip-Flop Static*

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5. *CMOS D Flip-FlopDynamic*

The dynamic CMOS D flip-flop design uses a dynamic logic technique to increase the flip-flop's speed and power consumption while storing data using a pair of cross-coupled inverters. Among the many benefits of the dynamic CMOS D flip-flop are its high speed, low power consumption, and small size. However, compared to the conventional CMOS D flip-flop, the dynamic CMOS D flip-flop can be more difficult to develop and produce.

III. PROPOSEDMETHOD

a. ***D F lip-Flop:*** Compared to its CMOS equivalent, the Fin-FET-based D Flip-Flop will be more energy-efficient due to its substantially lower power consumption. Furthermore, Fin-FETs' improved gate control will guarantee quicker.
enhanced noise immunity and faster switching speeds, which support system stability.

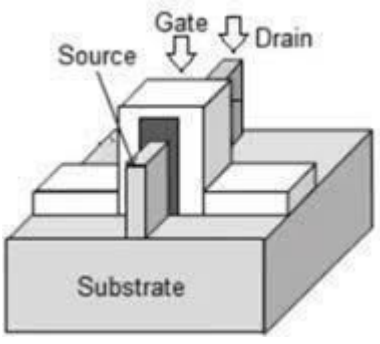
b. ***Asynchronous Up and Down Counters:*** Fin-FETs will improve performance and lower power dissipation in asynchronous up and down counters.
These counters will be able to function effectively at smaller technology nodes thanks to Fin-FETs' improved scalability. Furthermore, the counters will operate dependably in noisy settings thanks to the noise level reduction.

c. ***Reduced Power Consumption :*** As CMOS technology shrinks, leakage currents increase, leading to higher static Power dissipation. In contrast ,FinFETtechnology minimizes these leakage currents, which results in up to 57% lower power consumption compared to CMOS. This energy efficiency is crucial for battery-powered devices such as smart phones and portable electronics, where low power consumption is essential for longer battery life.

d. ***Improved Noise Immunity:*** One of the challenges with smaller CMOS transistors is reduced noise immunity, which can lead to instability in circuits, particularly at High speeds. The unique three-dimensional structure of F in FETs provides superior noise immunity by improving gate control and reducing the impact of noise, ensuring that digital circuits remain stable even in high-speed operations.

e. ***Enhanced Scalability:*** Below 20nm, planar CMOS transistors experience several issues, including short-channel effects and difficulty in controlling the transistor channel. F in FETs, however, maintain excellent scalability at these smaller nodes due to their three-dimensional structure. The ability to scale efficiently allows F in FET s to continue performing well as semiconductor manufacturing progresses, addressing the challenges that CMOS faces in advanced process nodes.

Fig:2Fin-FET



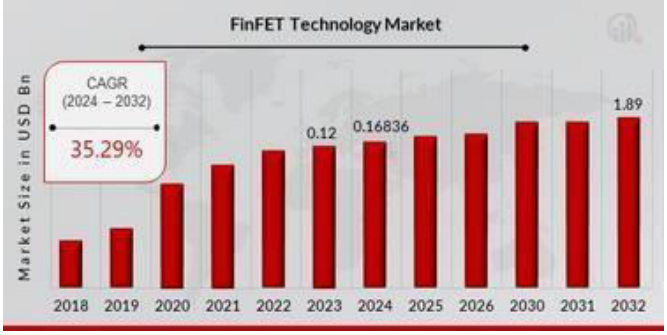
f. ***Higher Performance:*** The improved gate control in F in FET technology reduces short-channel effects, enhancing the overall performance of digital circuits. With faster switching speeds, F in FET-based circuits can operate at higher frequencies, supporting the design of high-speed, high-performance systems such as microprocessors and digital signal processors (DSPs). Additionally, this increased performance makes F in FET a strong contender for use in Internet of Things (IoT) applications, where both speed and energy efficiency are critical.

g. ***Reduced Leakage Current:*** The F in FET structure minimizes subthreshold leakage, gate leakage.

h. ***Better Performance in High-Frequency Applications***: The F in FET-based system ensures stable performance in GHz-range circuits.

i. ***Faster, More Reliable, and More Energy-Efficient System:*** The proposed F in FET-based Flip-Flop and Counter design ensures high-speed operation, lower power usage, and improved reliability compared to conventional CMOS-based designs.

Graph:1GrowthofFin-FETinFuture



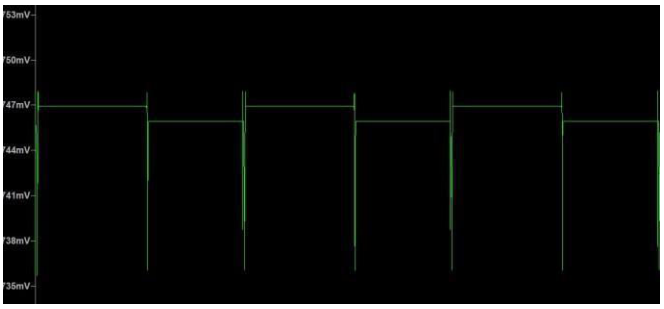
The above graph about the growth of Fin-FET in the past, present and future also. The growth of Fin-FET is high in 2032.

Table1:TableofcomparisonbetweenCMOSandFin-FET :

Parameter	CMOS technology	Fin-FET technology
Structure	Planar, Single Gate MOSFET	3DStructure, Double Gate for Better control
Short-Channel Effects(SCEs)	Severe at advanced nodes	Strong Suppression of SCEs
Gate Control	Weak(single gate control)	Strong(Do Uble gate control)
Noise Immunity	Lower, more Susceptible to noise	Higher, better noise tolerance

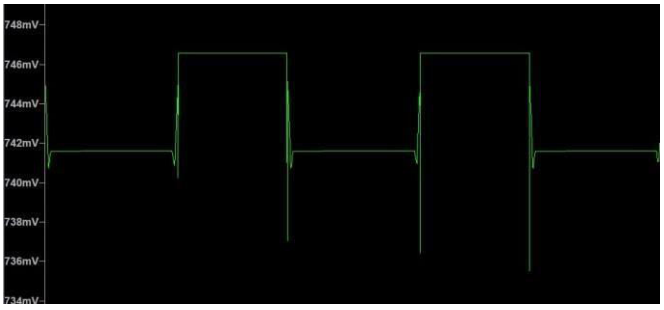
IV. RESULTSANDDISCUSSION

Fig:3:Fin-FETbasedonAsynchronousdowncounter



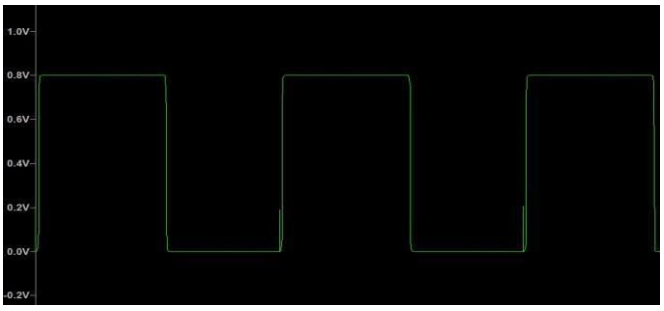
An asynchronous down counter is a type of counter that decrements its count with each clock pulse. It is called "asynchronous" because the flip- flops that make up the counter do not all change state at the same time—each flip-flop is triggered by the previous one's output rather than a common clock signal.

Fig4:Asynchronousupcounter



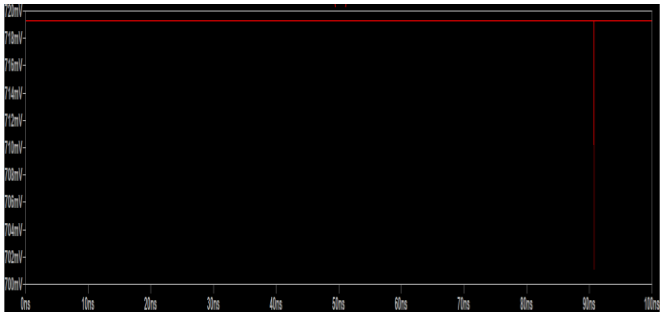
An asynchronous up counter is a type of digital circuit that counts up wards in binary, incrementing its count with each clock pulse.

Fig:5:Fin-FetBasedDFlip-Flop



A F in FET D Flip-Flop is a sequential circuit designed using Fin Field-Effect Transistors (F in FETs) instead of traditional CMOS transistors.

Fig:6.Johnsoncounter



A Johnson Counter, also known as a Twisted Ring Counter, is a type of shift register counter where the complemented output of the last flip-flop is fed back as input to the first flip-flop.

V. CONCLUSION

Traditional CMOS-based circuits encounter several difficulties as semiconductor technology continues to advance, such as high power consumption, elevated leakage currents, and short-channel effects. In order to show the superiority of Double Gate (DG) F in FET technology over traditional CMOS technology, this study investigated the design and implementation of high-speed, low-power CMOS D Flip-Flops and counters. The potential of Fin-FET for energy-efficient digital applications is demonstrated by the 57.13% reduction in power consumption and the 46.02% reduction in noise. Using Fin-FET technology to build True Single-Phase Clock (TSPC) D Flip-Flops, Johnson Counters, and asynchronous up/down counters showed that it is possible to achieve high- speed operations with low power dissipation.

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